

NOTES, UNLESS OTHERWISE SPECIFIED:

- 1. The netname "P3P3V" represents connection to the +3.3V digital power plane.
- 2. The netname "P1P8V" represents connection to the +1.8V digital power plane.
- 3. The netname "P1P1V" represents connection to the +1.1V digital power plane.
- 4. The symbol ⚡ represents connection to the digital ground plane.
- 5. A "Z" suffix on a signal name indicates an active low signal.
- 6. A "\_S" suffix on a signal name indicates a trace that is between a driver and a series termination resistor.
- 7. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
- 8. The letters DNI near a part mean "do not install".

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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	Initial Release		
B	Corrected 1.1V and 1.8V enables to regulator		

Z PCB1

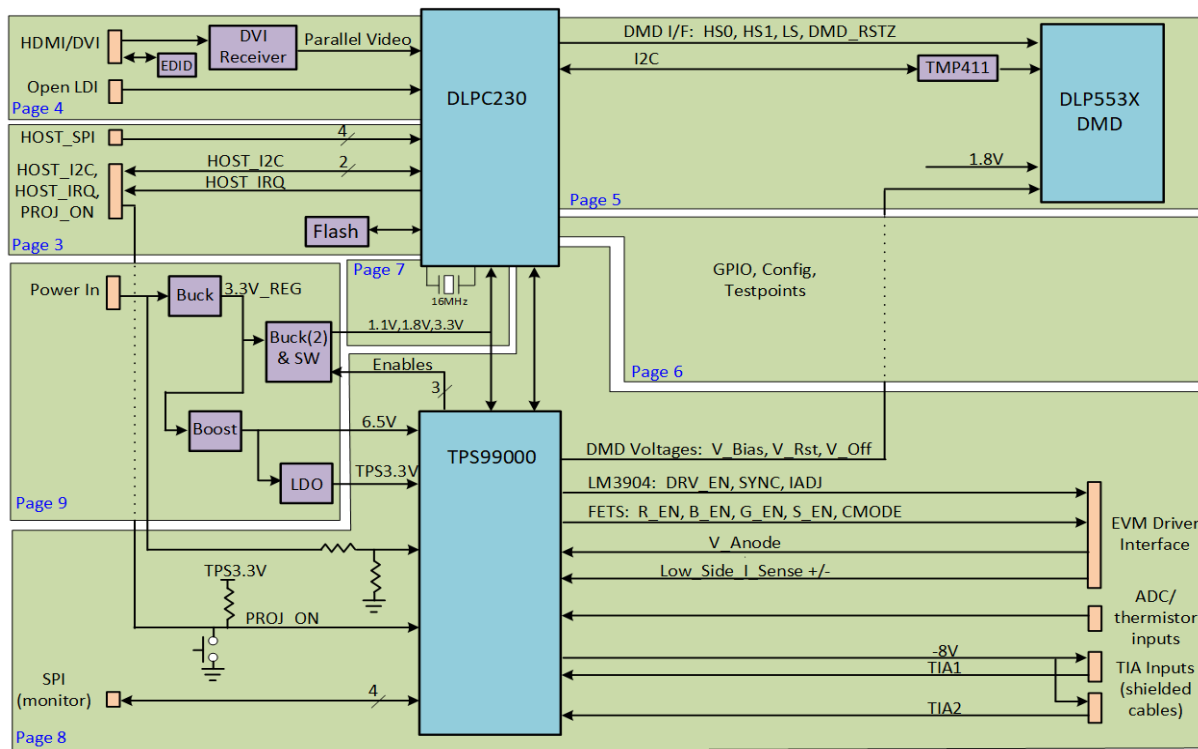


PCB, DLP553X Controller  
DLP033B

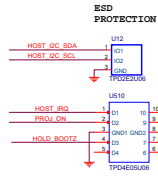
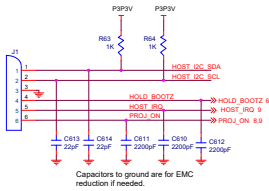


TEXAS INSTRUMENTS

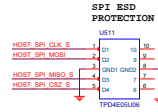
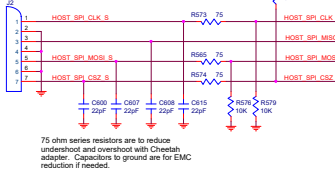
OWN George Pawlowski		DATE 4/13/2019		TEXAS INSTRUMENTS	
DRAWN		EVAL		(C) COPYRIGHT 2017 TEXAS INSTRUMENTS ALL RIGHTS RESERVED	
EVAL		REV		TITLE	
REV		REV		DLP553x EVM Controller	
NEXT ASSY		USED ON		D DRAWING NO DLP033	
APPLICATION		REV Cadence Capture 16.6		REV B	
				SCALE	
				SHEET 1 of 9	



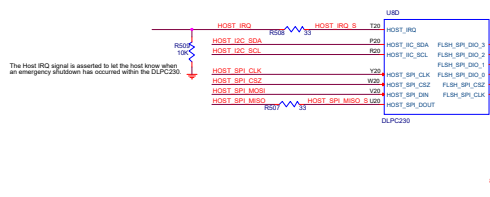
# HOST I2C, PROJ\_ON, IRQ, HOLD\_BOOT CONNECTOR



## HOST SPI CONNECTOR

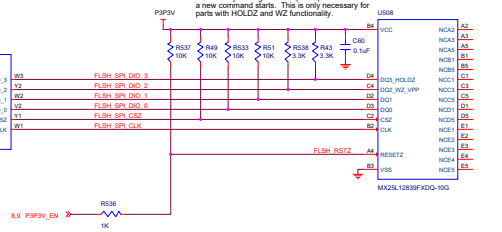


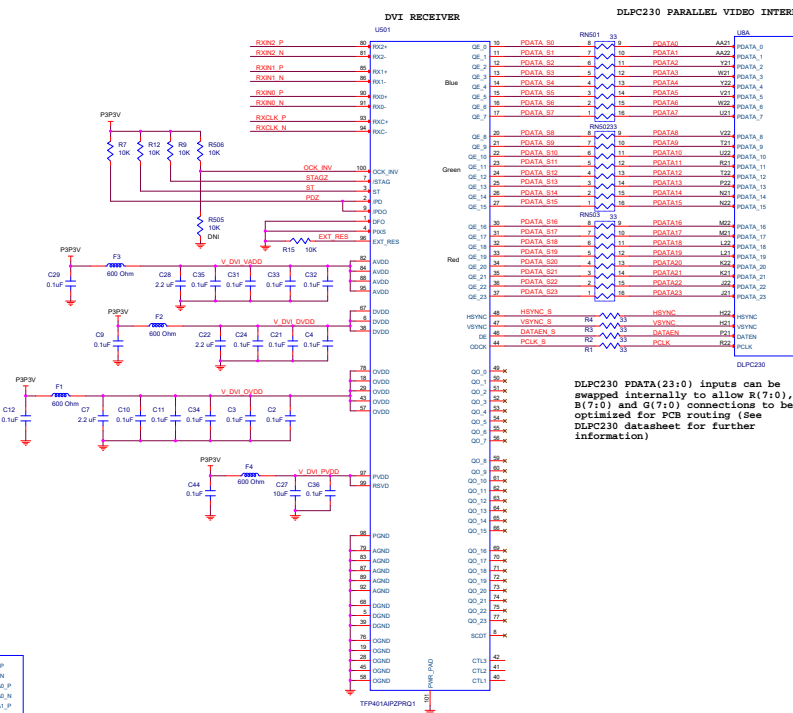
## DLP230 HOST INTERFACE



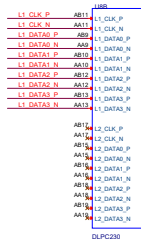
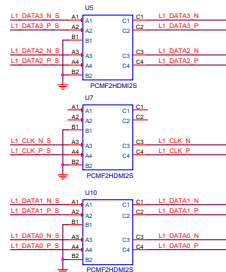
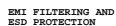
## DLP230 CONFIGURATION FLASH

DQ2 and DQ3 have smaller pullup resistors to ensure they are high after a quad operation before a new command starts. This is only necessary for parts with HOLD2 and V2 functionality.

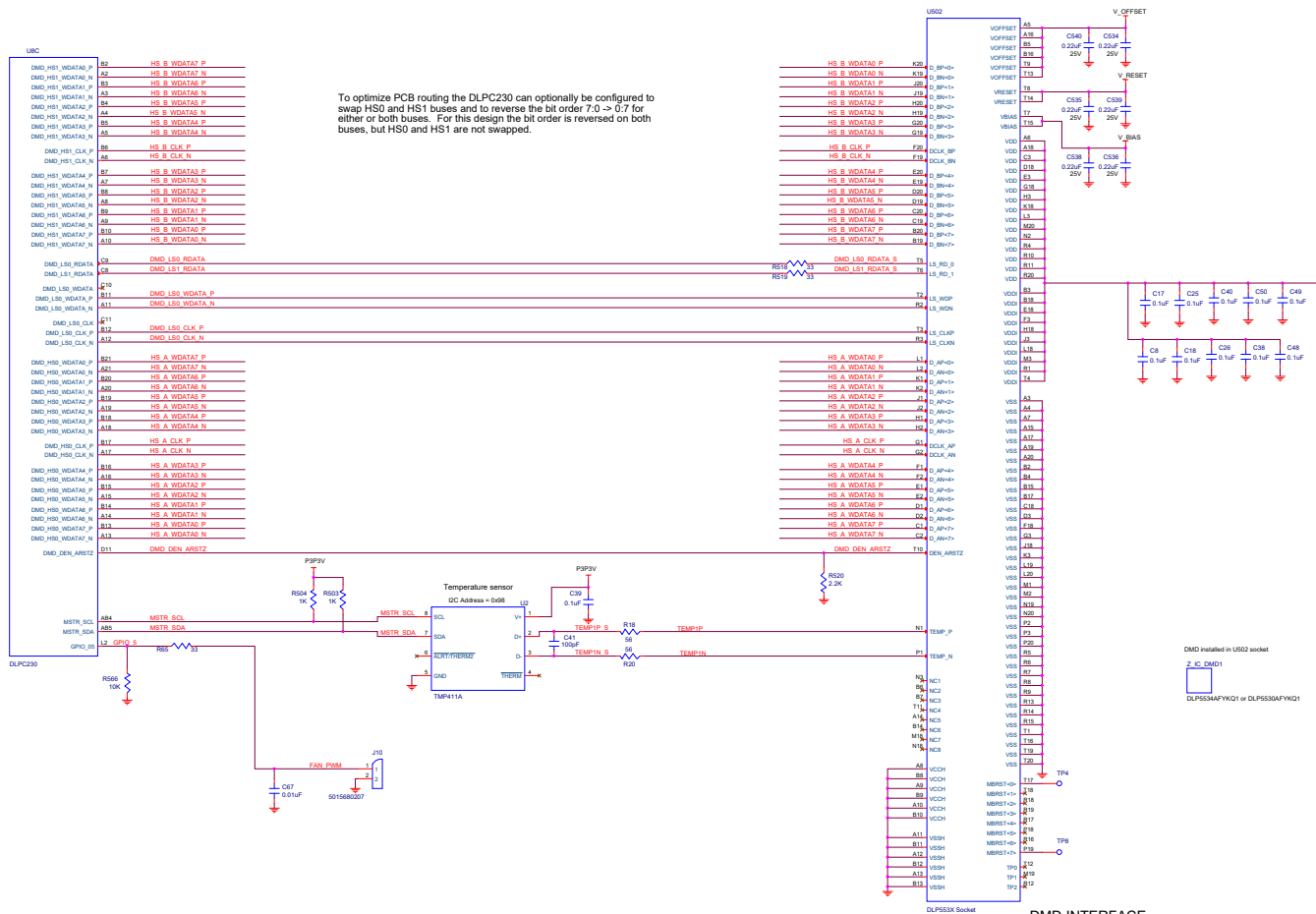




DLPC230 PDATA(23:0) inputs can be swapped internally to allow R(7:0), B(7:0) and G(7:0) connections to be optimized for PCB routing (See DLPC230 datasheet for further information)



To optimize PCB routing the DLPC230 can optionally be configured to swap HS0 and HS1 buses and to reverse the bit order 7:0 -> 0:7 for either or both buses. For this design the bit order is reversed on both buses, but HS0 and HS1 are not swapped.

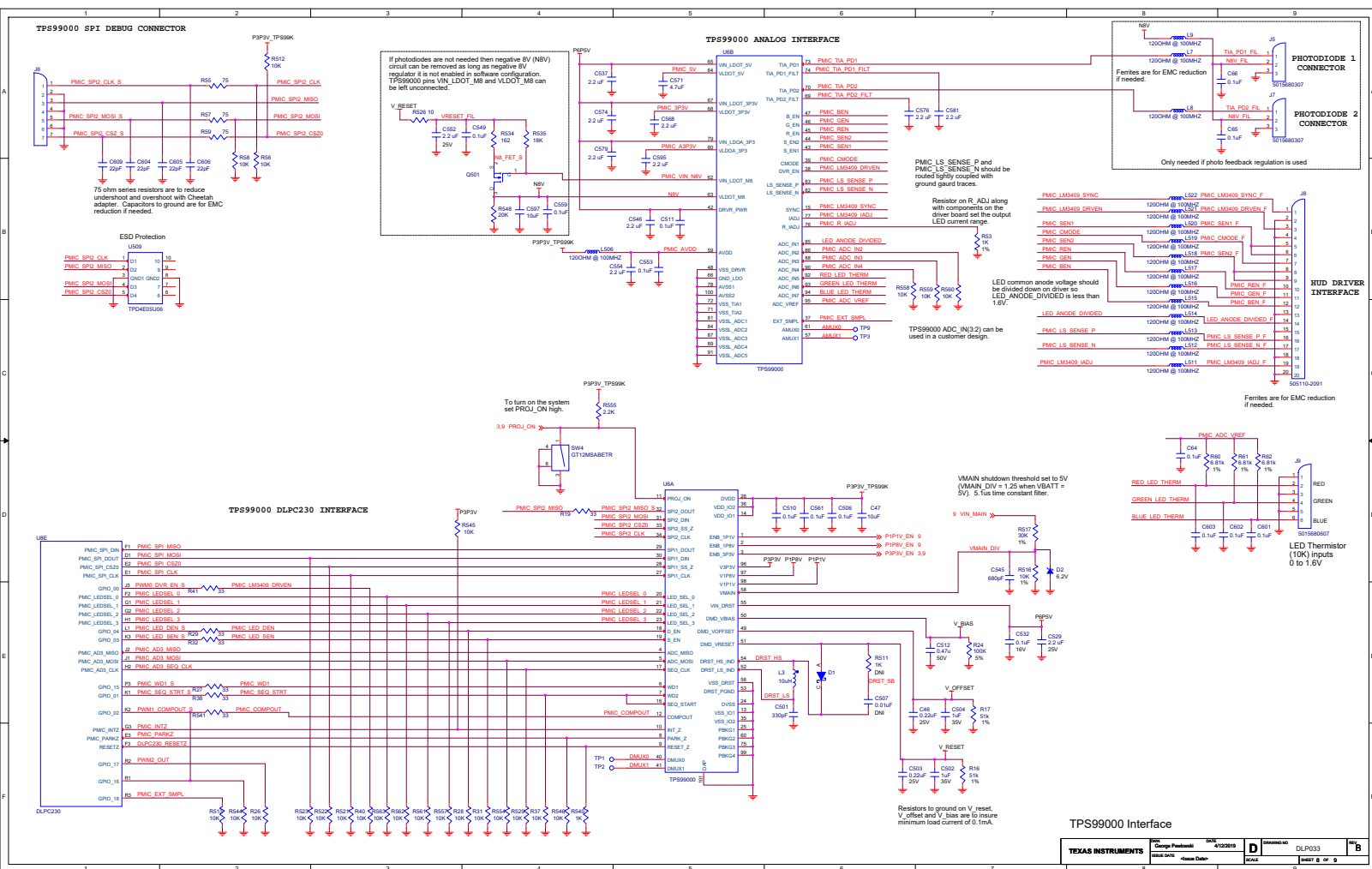


# DMD INTERFACE

TEXAS INSTRUMENTS	Device Pinout	41239110	D	DLPC230	8
	Device Pinout	Device Pinout	Device Pinout	Device Pinout	Device Pinout









# INPUT VOLTAGE FROM DRIVER

VIN\_MAIN 8  
VIN\_MAIN to TPS99000 to detect voltage dropping to park DMD. Assumes there is at least 400uF capacitance on driver board.

## 3.3V REGULATOR

## TPS99000 6.5V REGULATOR

## TPS99000 ANALOG 3.3V REGULATOR

## STATUS LEDS

## 3.3V SWITCH

## 1.8V and 1.1V REGULATORS

## SYSTEM POWER